Neuromorphic Computing with Nanoscale Spintronic Devices

Overview

In recent times, neuromorphic computing has emerged as a prominent technology for the post-Moore's era. Neuromorphic device engineering includes the evolution of components whose functions are similar to those of the human brain. Neuromorphic computing systems incorporate massive parallelism, high energy efficiency, and tolerance to fault and variations. They consume less power and processing memory. Conventional CMOS technology has been used for implementing neuromorphic computing in the past few decades. However, it has major disadvantages such as high energy consumption, high leakage, and restricted computing capacity. For large-scale hardware implementation of an efficient neuromorphic system, a lot of efforts have been made to realize artificial neurons and synapses using post-CMOS devices. An extensive research in low-power nanoscale devices is going on that can imitate the basic functionalities of biological neurons and synapses. The tremendous efforts have also been made to develop a neuron based on emerging devices such as resistive-RAM (RRAM), memristors, phase change memory (PCM), and magneto-resistive random access memory (MRAM). Spintronics has an enormous potential to provide very low power dissipation devices for neuromorphic computing. Spintronic devices have the ability to store information in the form of magnetization direction which can be retained almost indefinitely. The introduction of spintronic devices has made the implementation of analog neural networks possible with the advantages of high speed, low power consumption, and compact design.

This course will expose the participants to the fundamentals of neuromorphic computing, existing challenges in large-scale implementation of neural networks and solutions using novel devices, fundamentals of spintronic devices, spintronics-based neuromorphic computing architectures and their advantages over other technologies, and the simulation software tools through hands-on experience. Course participants will learn these topics through lectures and hands-on experiments. Also, the case studies will be shared to stimulate the research motivation of participants.

MHRD Scheme on Global Initiative on Academic Network (GIAN)

Course Duration:
December 19, 2022 – December 23, 2022

Course Organized By:
Department of Electronics and Communication Engineering, Indian Institute of Technology Roorkee, Roorkee, Uttarakhand, India.

Course Co-ordinator

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Course Registration

Course Registration Details	The participation fees for taking the course is as follows: **Participants from abroad : US $250** **Industry/ Research Organizations: INR 5000** **Academic Institutions (Faculty): INR 3000** **Academic Institutions (Students): INR 2000** The above fee includes all instructional materials, computer use for tutorials, laboratory equipment usage charges, 24 hrs free internet facility. The participants will be provided with accommodation on a payment basis. **Number of participants for the course will be limited to 100**
You Should Attend If…	• you are an executive, engineer, or researcher from manufacturing, service, and government organization including R&D laboratories. • you are a student (BTech/MSc/MTech/PhD) or faculty from a reputed academic and technical institution.

The Faculty

Abhronil Sengupta is an Assistant Professor in the School of Electrical Engineering and Computer Science at Penn State University and holds the Joseph R. and Janice M. Monkowski Career Development Professorship. He received the PhD degree in Electrical and Computer Engineering from Purdue University in 2018 and the B.E. degree from Jadavpur University, India in 2013. He worked as a DAAD (German Academic Exchange Service) Fellow at the University of Hamburg, Germany in 2012, and as a graduate research intern at Circuit Research Labs, Intel Labs in 2016 and Facebook Reality Labs in 2017. He is pursuing an inter-disciplinary research agenda at the intersection of hardware and software across the stack of sensors, devices, circuits, systems and algorithms for enabling low-power event-driven cognitive intelligence. Prof. Sengupta has published over 70 articles in referred journals and conferences and holds 4 granted/pending US patents. He serves on the IEEE Circuits and Systems Society Technical Committee on Neural Systems and Applications, Editorial Board of Neuromorphic Computing and Engineering, Frontiers in Neuroscience journals and the Technical Program Committee of several international conferences like DAC, ICCAD, ISLPED, ISQED, AICAS, ICONS, GLSVLSI and VLSID. He has been awarded the IEEE Circuits and Systems Society (CASS) Outstanding Young Author Award (2019), IEEE SiPS Best Paper Award (2018), Schmidt Science Fellows Award nominee (2017), Bilsland Dissertation Fellowship (2017), CSPIN Student Presenter Award (2015), Birck Fellowship (2013), the DAAD WISE Fellowship (2012). His work on neuromorphic computing has been highlighted in media by MIT Technology Review, ZDNet, US Department of Defense, American Institute of Physics, IEEE Spectrum, Nature Materials, among others. Prof. Sengupta is a member of the IEEE Electron Devices Society (EDS) and Circuits and Systems (CAS) Society, the Association for Computing Machinery (ACM) and the American Physical Society (APS).

Brajesh Kumar Kaushik received Doctorate of Philosophy (Ph.D.) in 2007 from Indian Institute of Technology, Roorkee, India. He joined Department of Electronics and Communication Engineering, Indian Institute of Technology, Roorkee, as Assistant Professor in December 2009; promoted to Associate Professor in April 2014; and since Aug 2020 he has been serving as full Professor. He had been Visiting Professor at TU-Dortmund, Germany in 2017; McGill University, Canada in 2018, and Liaocheng University, China in 2018. Prof. Kaushik is a Senior Member of IEEE and a member of many expert committees constituted by government and non-government organizations. He is currently serving as Distinguished Lecturer (DL) of IEEE Electron Devices Society (EDS) to offer EDS Chapters with quality lectures in his research domain. He is an Editor of IEEE Transactions on Electron Devices; Associate Editor of IEEE Sensors Journal; Associate Editor of IET Circuits, Devices & Systems; Editor of Microelectronics Journal, Elsevier; Editorial Board member of Journal of Engineering, Design and Technology, Emerald and Circuit World, Emerald. He is among the top 2% scientists in the world as per the Stanford University report of 2019. He is currently serving as a member of two technical committees namely, Spintronics (TC-5), and Quantum Computing, Neuromorphic Computing and Unconventional Computing (TC-16) of IEEE Nanotechnology Council. He is also the Regional coordinator (R10) of IEEE Nanotechnology Council Chapters. He has 12 books to his credit published by reputed publishers such as CRC Press, Springer, Artech, and Elsevier. He has been offered fellowships and awards from DAAD, Shastri Indo Canadian Institute (SICI), ASEM Duo, United States-India Educational Foundation (Fulbright-Nehru Academic and Professional Excellence). His research interests are in the areas of high-speed interconnects, carbon nanotube-based designs, organic electronics, device circuit co-design, optics & photonics-based devices, image processing, spintronics-based devices, circuits and computing.