✧ Selection and Mode of Payment:

Selected candidates will be intimated through E-Mail. They have to remit the necessary course fee to the Bank as per the details given below.

Outstation participants requiring accommodation and boarding facilities have to pay Rs. 2,000/- in addition to the course fee.

Account Name	GIAN NITW
Account No	**62447453600**
BANK	**State Bank of India**
Branch	**REC Warangal (NIT Campus)**
Branch Code	20149
IFSC Code	SBIN0020149
REC Warangal (NIT Campus)	**506004011**

Candidates registering early will be given preference in short listing process. For any queries regarding registration of the course, please contact the Course Coordinators:

Dr. P. Sreehari Rao
Department of Electronics and Communication Engineering, NIT, Warangal – 506004, Telangana
Tel: +91 8702462439 (O)
+91 9441342324
Email: patri@nitw.ac.in;
patri.srihari@gmail.com

✧ About GIAN Course:

Ministry of Human Resource Development (MHRD), Government of India (GoI) has launched an innovative program titled "Global Initiative of Academic Networks (GIAN)" in higher Education, in order to garner the best international experience. As part of this, internationally renowned Academicians and Scientists are invited to augment the Country's academic resources, accelerate the pace of quality reforms and elevate India's scientific and technological capacity to global excellence.

✧ About the Institute and Warangal:

National Institute of Technology, Warangal (NITW) formerly known as RECW is the first among seventeen RECs set up in 1959. Over the years, the Institute has established itself as a premier Institution in imparting technical education of a very high standard, leading to B.Tech, M.Tech and Ph.D. programmes in various specializations of Science and Engineering streams. Warangal is known for its rich historical and cultural heritage. It is situated at a distance of 140 km from Hyderabad. Warangal is well connected by rail and road. National Institute of Technology, Warangal campus is 3 km away from Kazipet railway station and 12 km away from Warangal railway station.

✧ About the Department

The Department of Electronics and Communication Engineering offers an Undergraduate program in Electronics and communication Engineering and three Postgraduate programs in EI, VLSI, and ACS Specializations. The Department has experienced faculty and well-established laboratories. The Department has liaison with reputed industries and R&D organizations like DRDO, ISRO ECIL, Analog Devices Bangalore and C-DAC.

GIAN GLOBAL INITIATIVE OF ACADEMIC NETWORKS

MHRD Govt. of India

Five Days GIAN Course on

Design and Implementation of Smart Internet-of-Things (IoT) Systems

~~ADVANCED CMOS CLOCK GENERATION CIRCUITS~~

December 21st~~5th~~ - 25~~9~~th , 2020~~17~~

Call for Registration and Participation

International Faculty

Dr. ~~Pavankumar Hanumolu~~Srinivas Katkoori
~~Associate Professor~~
~~Department of ECE~~
~~University of Illinois, Urbana-Champaign~~University of South Florida

Principal Coordinator
Dr. Sreehari Rao Patri

Co-Cordinator
Dr~~Sri~~ PMuralidhar

Department of Electronics and Communication Engineering,
National Institute of Technology Warangal
506 004, Telangana, India

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- **Overview of the Course:**

Internet-of-Things (IoT) is an ongoing technology transition with the goal of *connect the unconnected*. It has the great promise of positively changing the way humans live on this planet. IoT application domains are varied and diverse. Some examples are smart healthcare, smart transportation, smart home, smart farming, etc. There are three key technologies that are fueling the IoT revolution. First, is the fast and cheap computing, second, is the fast and high bandwidth communication and networking technologies, and third is the intelligent algorithms. Any IoT system architecture has at least three layers: edge layer, communication layer, and application layer. In the edge layer, smart edge nodes collect and filter data of interest. The collected data is then transmitted to the application layer through the communication layer. Typically, the communication layer consists of established communication network such as Internet or Wi-Fi. The application layer is housed at a data center where software applications are run to process the collected data and extract information that can aid in intelligent decision making.

In this course, the students will learn about the conceptual architecture of an IoT application, the design challenges, the enabling IoT technologies (edge computing, fog computing, communication technologies, and data analytics), and two case studies. The students will have hands-on experience with IoT hardware and software in the form of tutorials and lab assignments.

~~Phase-locked loops (PLLs) are de-facto clock generators ranging from MHz to GHz in digital, analog, and communication systems. They are used to: (i) generate clocks across a wide range of frequencies (MHz to GHz), (ii) clean-up noisy clocks, (iii) perform clock recovery, and (iv) provide frequency/phase modulation. In all these applications, they take up valuable resources in terms of area and power. PLLs have been conventionally implemented using analog architectures such as the charge-pump topology. Because they consume large area and are sensitive to transistor imperfections, more recently they are being realized using mostly digital architectures. It forms an integral part of modern CMOS deep micron~~ designs. They can be classified as digital and Analog

✧ International Faculty:

Dr. Srinivas Katkoori is a Computer Science and Engineering faculty at the University of South Florida (USF), Tampa, FL. His research group has been actively conducting research on related topics such as low power digital VLSI design, reliable system design, Internet-of-Things (IoT), smart embedded systems, smart transportation, smart healthcare, etc. Dr. Katkoori has directed 15 doctoral dissertations and 40 Master's Theses in the general discipline of Embedded Systems Design and Optimization. Dr. Katkoori serves on technical committees of several VLSI and embedded conferences and is a peer reviewer for many smart embedded systems journals and conferences. To date, he published over 125 peer-reviewed journal and conference papers. Three papers he has co-authored were nominated for best paper awards at 2003 ASP-DAC, 2014 IFIP/IEEE VLSI SOC, and 2019 AsianHOST conferences. Among notable professional service, Dr. Katkoori served on ACM SIGDA Board (2010- 2013) as Treasurer, as an Associate Editor of IEEE Transactions on VLSI (2006-10), and since 2015, he is serving as the vice-chair of IFIP Working Group 10.5 on Design and Engineering of Electronic Systems. Dr. Katkoori served as the General Chair of the 2019 2nd IFIP IoT Conference and 2020 IEEE International Symposium of Electronic Systems. Dr. Katkoori received his Ph.D. degree from the University of Cincinnati in 1998. He is a senior member of ACM and IEEE. ~~**Dr Pavankumar Hanumolu** is Associate Professor at Department of ECE , University of Illinois, Urbana-Champaign. Prof Hanumolu's research and teaching experience spanned over several years. Before this position, Dr Hanumolu was faculty of school of EECS, Oregon State University, Corvallis, OR USA for 7 years. He authored over 60 peer reviewed publications especially in IEEE transactions on solid~~

✧ Who can participate?

This program is open to the Faculty, Post graduate students, Engineers from industry , Research Scholars working in the relevant areas and scientists at R&D laboratories..

✧ How to Register?

Stage-1: Web Portal Registration:
Visit http://www.gian.iitkgp.ac.in/GREGN/index and create login User ID and Password. Fill up the blank registration form and do web registration by paying Rs. 500/- online through Net Banking / Debit / Credit card. This provides the user with life time registration to ~~enrol~~enroll in any number of GIAN courses offered.

Stage-2: Course Registration:
Login to the GIAN portal with the user ID and Password already created in Step 1. Click on Course Registration option at the top of Registration Form. Select the Course titled "**Design and Implementation of Smart Internet-of-Things (IoT) Systems~~ADVANCED CMOS CLOCK GENERATION CIRCUITS~~**" from the list and click on Save option. Confirm your registration by clicking on Confirm Course.

✧ Registration Fee:

Faculty	**Rs. 2,000/-**
Participants from Industry / Research organizations	**Rs. 4,000/-**
Students & Scholars Without award of grade With award of Grade	 Rs 500/- Rs 1,000/-
Participants from abroad	**US $ 200**

The Registration fee includes instructional materials, laboratory use and session teas.

The out-station participants will be provided with boarding and lodging on additional payment of Rs. 2,000/- in Student Hostel on sharing basis

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