GLOBAL INITIATIVE OF ACADEMIC NETWORKS
(GIAN)

Ministry of Human Resource Development
Government of India

GIAN COURSE
ON
HIGH PERFORMANCE COMPUTING CONCEPTS AND PRACTICE
08-13 OCTOBER 2018

http://www.riken.jp/en/about/intro/

COURSE COORDINATOR : Dr. P. B JAYARAJ

Organized by
Department of Computer Science & Engineering
National Institute of Technology Calicut
Calicut 673601 Kerala

HIGH PERFORMANCE COMPUTING CONCEPTS AND PRACTICE

Course Overview

High performance computing (HPC) is central to all walks of science and engineering, emerging as a game changing tool in breakthrough research and engineering. It is central to the design of new materials and products endowed with properties such as energy efficiency, environmental compatibility and manufacturability. It is central to our ability to combat natural and biological disasters, as well as secure critical resources such as clean air and water for future generations. Given that a nation's strategic advantage is measured by its standing in HPC, timely investment in HPC education emphasizing modern concepts and practice is key to maintaining India's relevance and competitiveness on the world stage.

A modern course in this area must include a broad conceptual basis that allows the creation of HPC software that is both correct as well as performs well. Unfortunately, with the cessation of improvements in transistor performance and clock frequency scaling, achieving high energy efficiency and performance requires techniques that allow the use of CPUs as well as a growing number of accelerators such as GPUs, FPGAs, as well as coprocessors such as the Xeon Phi. All existing leading HPC systems as well as the proposed pre-Exascale machines incorporate such heterogeneous architectures. Unfortunately, programs written for such heterogeneous systems are extremely difficult to debug as well as tune for performance.

This workshop will introduce faculty and researchers from technical institutions to the latest trend of using accelerators for high performance computing. It will provide incentives to seek and understand new computational approaches, enabling solutions that were unattainable previously. The course will be based on technology (hardware and software) readily available to all researchers, and mainly seeks to provide the know-how that is essential to put the technology to optimal and correct use.

Course Objective

The main objectives of the course are as follows:

1. To give an overview of parallel computing and its programming approaches suitable for different accelerators.
2. To concretely illustrate why and how parallel programming attains the desired levels of performance while ensuring correctness and staying within project schedules.
3. To learn how GPUs work and how they can be utilized for scientific programming
4. To enable the participants learn the latest trends in supercomputing.
5. To provide practical exposure by giving hands-on experiences in GPU, Xeon-Phi, MPI, OpenMP and GPU Programming
6. Course is driven through a single cohesive running example: an N-body simulation program.

COURSE MODULES

Module 1	**Basics of Parallel Programming** 1. Illustration of Parallel Computing using a pre-packaged application 2. Illustration of Amdahl's Law
Module 2	**MPI based parallel computing** 1. An N-body simulation in MPI 2. Verification of Correctness & Tuning for performance
Module 3	**OpenMP based parallel computing** 1. An N-body simulation in OpenMP 2. Verification of Correctness & Tuning for performance
Module 4	**GPU based parallel computing** 1. Constructs and their behaviour 2. Sample CUDA programs 3. An N-body simulation in CUDA
Module 5	**Accelerator based parallel computing** 1. Basics of Xeon-Phi programming 2. Different approaches to Xeon-Phi programming 3. Hands-on experience : Xeon Phi
Module 6	1. Advanced issues in HPC 2. The Exascale initiative

Registration Fees

Participants from abroad : US$ 200*

Participants from India:

- Industry/ Research organizations : Rs 8000/-*
- Faculty from Academic Institutions : Rs 4000/-*
- Research Scholars/Students : Rs 3000/-*

The registration fee includes the instructional materials, refreshments between sessions and working lunch. The accommodation will be provided to the outstation participants on payment basis subject to availability. Separate request is to be submitted in prior by participants for accommodation arrangement. TA/DA will not be paid for any participants.

*additional 18% GST is applicable to all above fees

Registration Process

Step 1 - Web Portal Registration:

Visit GIAN Website at the link: http://www.gian.iitkgp.ac.in/GREGN/index and create login, User ID, and Password. Fill up the GIAN registration form and do web registration by paying Rs 500/- online through Net Banking/ Debit/ Credit Card as per instructions given there in. This provides the user with life time registration to enroll in any number of GIAN courses offered (skip this step if already registered with GIAN portal).

Step 2 - Course Registration:

Login to the GIAN portal again with the user ID and password already created in Step 1. Click on course registration option at the top of registration form. Select the course titled *High Performance Computing Concepts and Practice* from the list and click on the Save option. Confirm your registration by clicking on the Confirm Course option. The participant may then proceed for the course registration with the course coordinator by filling out the registration form and paying the course registration fee. The course fee should be paid in the form of Draft/NEFT/RTGS. The account details are given below. The duly filled up registration form and the DD/ NEFT/RTGS receipt must be sent to the course coordinator. For provisional registration, scanned copies of the above documents can be sent to jayarajpb@nitc.ac.in. The DD/Receipt of NEFT/RTGS and the original registration form (hard copy) must reach the coordinator on or before 02 June 2018. The maximum number of participants of the program would be limited to 50.

Account Name	DIRECTOR NIT CALICUT
Account No.	35909407299
Bank	State Bank of India
Branch	CREC, Chathamangalam,Kozhikode
Branch Code	002207
IFSC	SBIN0002207
MICR Code	673002012
SWIFT Code	SBINPN BB392

Important Dates

Last date for receiving applications: 15th Sept. 2018
Last date for Intimation to Participants by email: 25th Sept. 2018
Course Dates: 8-13 Oct 2018

About GIAN Course

MHRD, Govt. of India has launched an innovative program titled Global Initiative of Academic Networks (GIAN) in higher Education, in order to garner the best international experience. As part of this, internationally renowned Academicians and Scientists are invited to augment the Country's academic resources, accelerate the pace of quality reforms and elevate India's scientific and technological capacity to global excellence.

About NIT Calicut

National Institute of Technology Calicut (NITC) is one of the 31 institutions of national importance governed by the NIT Act 2007 and is fully funded by the Government of India. Originally established in 1961 as a Regional Engineering College (REC), it was transformed into a National Institute of Technology in the year 2002. The institute offers bachelors, masters and doctoral degree programs in Engineering, Science, Technology and Management. With its proactive collaborations with a multitude of research organizations, academic institutions and industries, the institute has set a new style for its functioning under the NIT regime. The Institute is presently offering ten UG programs and thirty PG programs along with Ph.D programme in various fields of Engineering, Science and Technology.

About the Department of CSE NITC

The CSE Department offers undergraduate programme in Comptuer Science and Engineering, graduate programmes in Information security and Computer Science & Engineering and research programme leading to Ph.D. Degree. The major research activities are in the areas of Parallel and distributed Computing Systems, Intelligent Systems, Program Analysis, Algorithms and Complexity & Information Management and security. More details can be obtained from the departmental website at http://minerva.nitc.ac.in/cse/

HPC & Biocomputing Research Group

In order to contribute to the fascinating and emerging area of computational analysis of biological processes, the National Institute of Technology Calicut has established the HPC & Biocomputing Research Group in 2013. The research group consists of three faculty members from the Department of Computer Science and Engineering and 13 PhD scholars presently working in various domains. Since its inception, the group is lively engaged in the field of Computational biology and Biological data mining. HPC subgroup supplies the computing power for the bigdata compute-intesive operations. Recent works include the GPU based virtualscreening algorithms for fast drug discovery.

Address for Correspondence

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COURSE FACULTY

International Faculty

Dr. Ganesh Gopalakrishnan, Professor School of Computing University of Utah, USA http://www.cs.utah.edu/~ganesh/. Ganesh Gopalakrishnan has a Bachelor's degree in Electrical Engineering (REC Calicut (1978), an M.Tech. degree in Electronics (IIT Kanpur, 1980) and a PhD degree in Computer Science (Stony Brook University, New York, 1986). Over the last 31 years, he has been on faculty at the School of Computing, University of Utah, Salt Lake City, USA. He has graduated 21 PhD students to date, and is advising five more PhD students currently. His current projects from the National Science Foundation and Department of Energy in the USA cover Fault Tolerant Computing, Floating-point Precision Tuning, High-performance Computing, Data Race Detection of OpenMP programs, and Distributed Systems. Prof. Gopalakrishnan has been part of seven consecutive tutorials offered at the Supercomputing conference (2010 through 2016) where he lectured on debugging MPI and shared memory programs. He is an ACM Distinguished Scientist and a Senior Member of IEEE. Prof. Gopalakrishnan is also passionate about education at all levels, and has mentored 34 NSF Research Experience for Undergraduates (REU) students in the USA. His former students include three faculty members, and computer scientists at companies including Google, Amazon, Microsoft and Intel. He was General Chair of the 2011 Computer Aided Verification Conference, and is the lead organizer of a National Science Foundation workshop on Software Infrastructures for Sustained Innovation in February 2017. He is a co-author of the Department of Energy Report of the HPC Correctness Summit held in January 2017. He has published over 170 refereed conference and journal papers. He is author of a textbook Computation Engineering: Applied Automata Theory and Logic (Springer, 2006). He is Director of the Center for parallel computing at Utah.

Host Faculty

Jayaraj P B is Assistant Professor in the Department of Computer Science & Engineering, NIT Calicut having experience of about 12 years in Industry and Academia. He is currently the in-charge of a central facility of the institute namely Central Computer Centre which owns a 26 Teraflops 14 node Supercomputing facility. His area of research includes Parallel Computing, GPU Computing, Machine learning and Computational Intelligence. His major expertise includes Linux Kernel Programming and GPU CUDA programming. He has established state-of-the-art Hybrid (CPU-GPU) Supercomputing facility in Central Computer Centre at NIT Calicut. His current research area is computational drug discovery.