MHRD | Government of India
Ministry of Human Resource Development

सत्यमेव जयते

Global Initiative on Academic Network (GIAN)

Logic Design under Paradigm of Rebooting Computing

Overview

CMOS based computing is reaching its limits, and computation beyond Moore's law requires research explorations in (i) new materials, devices, and processes; (ii) new architectures and algorithms; (iii) new paradigm of logic bit representation. The focus is on the innovative ways to compute under the umbrella of rebooting computing such as spintronics, quantum computing, adiabatic, and reversible computing, etc. This course will provide an interdisciplinary review of rebooting computing methods especially quantum computing, spintronics, and reversible/adiabatic computing. Primarily, logic design of circuits under the paradigm of rebooting computing will be covered to enable faculty, graduate students, and industry participants to perform research and realize products.

The primary objectives of the course are as follows:

1. To develop fundamentals of rebooting computing.
2. To introduce principles of spintronics, quantum computing, adiabatic, and reversible computing.
3. Logic design of spintronics, quantum computing, adiabatic and reversible computing.
4. Programing skill development for spintronics, adiabatic and reversible computing, and quantum computing.
5. To analyze and debug circuits and architectures systems built in spintronics, quantum computing, adiabatic and reversible computing.
6. To develop understanding of the pros and cons of various emerging technologies in rebooting computing.

Course duration	December 25 – December 29, 2017 (5 days). Number of participants for the course will be limited to 30.
Who can attend	▪ Executives, engineers, and researchers from industry and government organizations including R&D laboratories. ▪ Students at all levels (BTech/MSc/MTech/PhD) ▪ Faculty from reputed academic and technical institutions.
Fees	The participation fees for taking the course is as follows: **Participants from abroad : US $150** **Industry/ Research Organizations: Rs. 5000** **Faculty: Rs. 3000** **Students: Rs. 2000** The above fee include all instructional materials, computer use for tutorials and assignments, laboratory equipment usage charges, 24 hours free internet facility. The participants will be provided with accommodation on payment basis.

The Faculty

Dr. Himanshu Thapliyal is an Assistant Professor and Endowed Robley D. Evans Faculty Fellow with the Department of Electrical and Computer Engineering, University of Kentucky, Lexington, KY, USA. He received the Ph.D. degree in Computer Science and Engineering from University of South Florida, Tampa, in 2011. From 2012 to 2014, he worked as a designer of processor test solutions at Qualcomm, where he received the Qualcomm QualStar Award for contributions to memory built-in self-tests. He has published over 100 journal/conference articles; and received Best Paper awards at 2012 IEEE Computer Society Annual Symposium on VLSI (ISVLSI) and 2017 Cyber and Information Security Research Conference (CISR). His research articles are among most downloaded articles in IEEE Transactions on VLSI, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, and IEEE Consumer Electronics Magazine; and are highlighted in the MIT Technology Review, ACM TechNews, etc. Dr. Thapliyal's research interests include emerging computing paradigms under rebooting computing, hardware assisted cybersecurity, and smart health. He is a Senior Member of IEEE. More details are available at http://hthapliyal.engineering.uky.edu/

Dr. Brajesh Kumar Kaushik received his Doctorate of Philosophy (Ph.D.) in 2007 from Indian Institute of Technology, Roorkee, India. He joined Department of Electronics and Communication Engineering, Indian Institute of Technology, Roorkee, as Assistant Professor in December 2009; and since April 2014 he has been an Associate Professor. He has served as General Chair, Technical Chair, and Keynote Speaker of many reputed international and national conferences. Dr. Kaushik is a *Senior Member* of IEEE and member of many expert committees constituted by government and non-government organizations. He is Associate Editor of *IET Circuits, Devices & Systems*; Editor of *Microelectronics Journal*, Elsevier; Editorial board member of *Journal of Engineering, Design and Technology*, Emerald; and Editor of *Journal of Electrical and Electronics Engineering Research*, Academic Journals. He also holds the position of Editor-in-Chief of *International Journal of VLSI Design & Communication Systems*, and *SciFed Journal of Spintronics & Quantum Electronics*. He has received many awards and recognitions from the International Biographical Center (IBC), Cambridge. His name has been listed in Marquis Who's Who in Science and Engineering® and Marquis Who's Who in the World®. Dr. Kaushik has been conferred with *Distinguished Lecturer* award of IEEE Electron Devices Society (EDS) to offer EDS Chapters with quality lectures in his research domain. His research interests are in the areas of high-speed interconnects, low-power VLSI design, memory design, carbon nanotube-based designs, organic electronics, FinFET device circuit co-design, electronic design automation (EDA), spintronics-based devices, circuits and computing, image processing, and optics & photonics based devices.

Course Co-ordinator

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