Guru Jambheshwar University of Science and Technology, Hisar

Organizes One Week

GIAN-MHRD, Government of India Sponsored Workshop-Course

On

"Authentication and Obfuscation of Integrated Circuits"

(From 28th Aug, 2017 to 1st Sep., 2017)

The focus of this course will be on hardware security. The failure to secure integrated circuit chips can result in loss of revenue due to reverse engineering, sale of recycled parts as new chips, wrong authentication of chips, sale of excess parts by untrusted foundries etc. Research on hardware prevention of wrongful authentication, piracy and intellectual property (IP) can be broadly classified into two main categories: 1) authentication-based approach or 2) obfuscation-based approach. The authentication-based approaches include physical unclonable functions (PUFs) based authentication, key locking and hardware metering. Obfuscation-based approach is a technique that transforms an application or a design into one that is functionally equivalent to the original but is significantly more difficult to reverse engineer. Some hardware protection methods are achieved by altering the human readability of the hardware description language (HDL) code or by encrypting the source code based on cryptographic techniques. Recently, a number of hardware protection schemes have been proposed that modify the finite-state machine (FSM) representations to obfuscate the circuits. This one week course will cover recent progress on topics such as PUFs (Physical unclonable functions) which can store secret keys in integrated circuits (ICs) by exploiting the uncontrollable randomness due to manufacturing process variations. These PUFs can be used for authentication of devices and for key generation in security applications. Obfuscation approaches can prevent sale of excess parts and increase the complexity of reverse engineering.

Schedule		Authentication and Obfuscation of Integrated Circuits
	1.	August 28, Monday
		Inauguration: 9:00 AM
		Lecture 1: 09:30 to 10:30 AM Physical Unclonable Functions (PUFs): delay based PUFs and Memory based PUFs.
		Lecture 2: 10:45 to 11:45 AM Physical Unclonable Functions (PUFs): delay based PUFs and Memory based PUFs.
		Tutorial 1: 2:00 to 4.00 PM Problem solving session with examples
	2.	August 29, Tuesday
		Lecture 3: 9:30 to10:30 AM Modelling PUFs by Machine Learning
		Lecture 4: 10:45 to 11:45 AM Modelling PUFs by Machine Learning
		Tutorial 2: 2:00 to 4.00 PM Problem solving session with examples
	3.	August 30, Wednesday
		Lecture 5: 9:30 to 10:30 AM Logic Encryption, Hardware Trojans
		Lecture 6: 10:45 to 11:45 AM Logic Encryption, Hardware Trojans

		Tutorial 3 : 2:00 to 4:00 PM Problem solving session with examples
		First Examination for participants.
	4.	August 31, Thursday
		Lecture 7: 9:30 to10:30 AM Digital Signal Processing Architectures
		Lecture 8: 10:45 to 11:45 PM Digital Signal Processing Architectures
		Tutorial 4 : 2:00 to 4 PM Problem solving session with examples
	5.	September 1, Friday
		Lecture 9: 9:30 to 10:30 AM Static and. Dynamic Functional DSP obfuscation
		Lecture 10: 10:45 to 11:45 PM Static and. Dynamic Functional DSP obfuscation
		01:00 PM to 01:30 PM Final Examination for participants.
		Valedictory Session: 02:00 to 02:30 PM
		Number of participants for the course will be limited to fifty.
You Should Attend If…		• Executives, engineers and researchers from manufacturing, service and government organizations including R&D laboratories. • Student at all levels (B.Tech/M.Sc./M.Tech./PhD.) or Faculty from reputed academic institutions and technical institutions.
Registration process and Fees		• The applicant are required to get themselves register on GIAN web portal (http://www.gian.iitkgp.ac.in) to apply for any number of GIAN courses as and when necessary. • The course registration fee is separate. The participation fees (Demand draft drawn in favour of Registrar, GJUS&T, Hisar or NEFT/RTGS at PNB A/c No. 4674000100036542 (IFSC : PUNB0467400) for taking the course is as follows: Participants from abroad : US $500 Participants from Industry : Rs. 10,000/- Participants from University/Institutions (Faculty) : Rs. 2,500/- Participants from University/Institutions (Students/Scholars) : Rs. 1,000/- • The above fee includes all instructional materials, computer use for tutorials and assignments, laboratory equipment usage charges, 24 hr free internet facility. The participants will be provided with accommodation on payment basis, subject to availability and have to bear their foods expenses on their own.

The Faculty

Foreign faculty

Prof. Keshab K Parhi received B.Tech. degree from the Indian Institute of Technology (IIT), Kharagpur in 1982, the M.S.E.E. degree from the University of Pennsylvania, Philadelphia in 1984, and the Ph.D. degree from the University of California, Berkeley in 1988. He has been with the University of Minnesota, Minneapolis, since 1988, where he is currently the Distinguished McKnight University Professor and Edgar F. Johnson Professor in the Department of Electrical and Computer Engineering. He has published over 550 papers, has authored the textbook VLSI Digital Signal Processing Systems (Wiley, 1999) and co-edited the reference book Digital Signal Processing for Multimedia Systems (Marcel Dekker, 1999). Dr. Parhi is widely recognized for his work on high-level transformations of iterative data-flow computations and for developing a formal theory of computing for design of digital signal processing systems. His current research addresses VLSI architecture design and implementation of signal processing, communications and biomedical systems, error control coder and cryptography architectures, high-speed transceivers, stochastic computing, secure computing, and molecular computing. He is also currently working on intelligent classification of biomedical signals and images, for applications such as seizure prediction and detection, schizophrenia classification, biomarkers for mental disorder, brain connectivity, and diabetic retinopathy screening. Dr. Parhi is the recipient of numerous awards including the 2013 Distinguished Alumnus Award from IIT, Kharagpur, the 2013 Graduate/Professional Teaching Award from the University of Minnesota, the 2012 Charles A. Desoer Technical Achievement award from the IEEE Circuits and Systems Society, the 2004 F. E. Terman award from the American Society of Engineering Education, the 2003 IEEE Kiyo Tomiyasu Technical Field Award, the 2001 IEEE W. R. G. Baker prize paper award, and a Golden Jubilee medal from the IEEE Circuits and Systems Society in 2000. He was elected a Fellow of IEEE in 1996. He served as the Editor-in-Chief of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS —PART I (2004-2005 term), as technical program co chair of the 1995 IEEE VLSI Signal Processing workshop and the 1996 ASAP conference, and as the general chair of the 2002 IEEE Workshop on Signal Processing Systems. He was a distinguished lecturer for the IEEE Circuits and Systems society during 1996-1998. He served as an elected member of the Board of Governors of the IEEE Circuits and Systems society from 2005 to 2007.

Course Coordinator

Prof. Sanjeev Kumar Dhull is Chairman, Department of Electronics and Communication Engineering, Guru Jambheshwar university of Science and Technology, Hisar, India. He did his B.E (ECE) from Mangalore University, Mangalore, Master of Technology from Panjab University, Chandigarh and Ph.D. from GJUS&T, Hisar. He joined GJUS&T as a faculty member in 2006, where he currently holds the position of Chairperson in Department of Electronics and Communication Engineering. His research areas are Adaptive Signal Processing, Speech Processing. In these areas he has supervised several graduates & Post graduates students. He had published more than 55 research papers and visited foreign countries Kuala Lumpur and Singapore under different scheme of govt. of India.

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GLOBAL INITIATIVE OF ACADEMIC NETWORKS

MHRD, GOVT. OF INDIA

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