# Near/sub-threshold circuits and architectures for microprocessors

## Overview

In this course, we will introduce recent and important techniques for designing ultra-low-power computing hardware (e.g., microprocessors) in near/sub-threshold digital circuits for creating ultralow-power Internet of the Things (IoT) devices. We will study techniques ranging across layers from transistors to gates to architectures. Those techniques aim to address three important challenges in near/sub-threshold voltage circuits, namely extreme variability, active leakage, and low computing throughput.

The course consists of five three-hour lectures, assignments, and a final exam.

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| **Dates for the Course** | **9th January 2017 to 13th January 2017** |
| **Host Institute** | **IIT Madras** |
| **No. of Credits** | **1** |
| **Maximum No. of Participants** | **60** |
| **You Should Attend If…** | ▪ You are a digital circuit designer who intends to familiarize yourself with the latest low-power digital circuits and architectures.<br>▪ You work on digital architectures and you intend to study their low-power implementations.<br>▪ You are interested in hardware implementation details of integrated circuits for IoT devices.<br>▪ You work in the general area of circuit design and you intend to familiarize yourself with recent trends in digital circuits and architectures for research or development. |
| **Course Registration Fees** | The participation fees for taking the course are as follows:<br>▪ **Student Participants:** Rs. 1,000/-<br>▪ **Faculty Participants:** Rs. 5,000/-<br>▪ **Government Research Organization Participants**: Rs. 10,000/-<br>▪ **Industry Participants:** Rs. 40,000/-<br><br>The above fee is towards participation in the course, the course material, computer use for tutorials and assignments, and laboratory equipment usage charges.<br><br>**Mode of payment: Demand draft in favour of "Registrar, IIT Madras" payable at Chennai**<br>The demand draft is to be sent to the Course Coordinator at the address given below. |
| **Accommodation** | The participants may be provided with hostel accommodation, depending on the availability, on payment basis. Request for hostel accommodation may be submitted through the link: http://hosteldine.iitm.ac.in/iitmhostel |

# Course Faculty

**Prof. Mingoo Seok** received the BS (with summa cum laude) in electrical engineering from Seoul National University, South Korea, in 2005, and the MS and PhD degree from the University of Michigan in 2007 and 2011, respectively, all in electrical engineering. He was a member of technical staff in Texas Instruments, Dallas in 2011. Since 2012, he has been an assistant professor in the Department of Electrical Engineering at Columbia University. His research interests include process/voltage/aging/thermal-variation-adaptive VLSI circuits and architectures, ultra-low-power system-on-chip (SoC) design for emerging embedded systems, machine-learning VLSI hardware, and non-conventional computing/processing hardware design. He received 1999 Distinguished Undergraduate Scholarship from the Korea Foundation for Advanced Studies, 2005 Doctoral Fellowship from the same organization, and 2008 Rackham Pre-Doctoral Fellowship from University of Michigan. He also won 2009 AMD/CICC Scholarship Award for picowatt voltage reference work and 2009 DAC/ISSCC Design Contest for the 35pW sensor platform design. He also won 2015 NSF CAREER award. He has been serving as an associate editor for IEEE Transactions on Circuits and 2 Systems I since 2013, and IEEE Transactions on Very Large Scale Integration (VLSI) Systems since 2015.

## Course Coordinator

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