Recent Advances in VLSI Testing and Design-for-Test: Timing Tests, Test Compression, Cell Aware Test and Adaptive

Overview

Electronics and computing are rapidly transforming society. Be it communication, security, quality of life, health or financial well-being; machines are increasingly being used for making decisions that influence individual and society. Consequently, it is imperative that the underlying electronic hardware perform correctly and be defect free. However, testing and screening electronic components to requisite "zero defect" standards is extremely challenging. This is due to the defectivity and manufacturing variability inherent in aggressively scaled nanometer IC technologies, and the staggering design complexities. At present, systems-on-chips (SOCs) incur 10-15% overheads for design-for-test (DFT) circuitry. Even so, defective parts frequently escape the testing process and cause unacceptable failure in operation. Developing improved test methodologies is a continuing and critical challenge for the microelectronics industry.

DFT methods for testing ICs and SOCs have seen significant advances, many of which have been adopted by industry, over the past decade. Because of the fast-paced development and the complexity, many of these new approaches are not well understood even by many test professionals, and are rarely taught at universities. Until the early 2000s, most digital ICs were tested using tradition scan based on the classical stuck-at fault model. High end microprocessors were additionally tested for timing. By early in the new millennium, delay faults were so frequently observed in complex ASICs and SOCs fabricated in advanced technologies that some form of cost effective timing tests became necessary. Soon low cost scan based structural delay tests, in particular Transition Delay Fault (TDF) tests, became an integral part of high quality test sets. To overcome the substantial increase in test set size and test costs, test compression DFT methodologies were devised. Within last decade, test compression has been widely adopted by industry in virtually every high end design. But challenges remain. In past 2-3 years, it has been observed that even the best industrial strength structural tests are failing to detect an alarming number of defective parts, resulting in nearly 1000 DPPM (0.1%) defects in microprocessor parts. This has focused interest on powerful new "cell aware" fault models that target layout defects missed by traditional test generation. Meanwhile, an emerging adaptive test methodology is being adopted to address the "zero defect" demands of the automobile industry and other critical applications.

This course aims at thorough understanding and effectiveness of four new DFT technologies – (1) timing and delay testing, (2) test compression, (3) adaptive testing and (4) cell aware test. The presentation will rely extensively on Industry data on processor, and smart phone SOC parts. The first third of the course will review test basics to facilitate a full understanding of the advanced material to follow. It may be noted that this material is not available in any current text book on testing. For details, please refer to MNIT website (http://mnit.ac.in)

Dates	**Course Duration** : **July 25 – 29, 2016** **Last date of Registration** : **July 20, 2016**
Modules	**Module 1: VLSI Test and Design-For-Test (DFT) Fundamentals (4 Lectures -8 hours)** **Module 2: Timing Tests for Delay Fault Detection and Speed Binning (2 Lectures -4 hours)** **Module 3: Test Compression and Logic BIST (1 Lecture -2 hours)** **Module 4: Cell Aware Tests and other Advanced Fault Models (1 Lecture -2 hours)** **Module 5: Adaptive Test Methods Targeting "Zero Defect" IC Quality (2 Lectures -4 hours)** **Number of participants for the course will be limited to fifty. Selection of participants shall be on "First Come First Served" basis only.**
You Should Attend If you are …	▪ Scientist with an interest in IC Design and Test ▪ VLSI Designers from Industry/researchers from Govt. organizations including R&D laboratories ▪ Faculty from reputed academic institutions and technical institutions. ▪ Students at all levels (BTech/MSc/MTech/PhD)

Registration Fees	**GIAN Portal registration fee : Rs 500 (mandatory for all participants).** 1. Create login and password at http://www.gian.iitkgp.ac.in/GREGN/index 2. Login and complete the Registration Form and select Course(s) 3. Confirm application and pay Rs. 500/- (non-refundable) through online payment gateway. 4. Download "pdf file" of the application form and email it to the Course Coordinator. 5. Once course coordinator shortlists the applicant, an email shall be sent to him/her. He/she may proceed for course registration as described in next section. **Registration Fee (exclusive of GIAN Portal Registration Fee)** **Participants from abroad : US $100** **Industry/ Research Organizations : Rs 5000** **Faculty from other Academic Institutions : Rs 3500** **Students from other Academic Institutions : Rs 1000** **Faculty /Students from MNIT and IIIT Kota : Rs 1000**
Course Registration	1. Fees may be paid via Demand Draft in favour of "REGISTRAR (SPONSORED RESEARCH) MNIT Jaipur" payable at Jaipur. OR Fees can be paid through National Electronic Funds Transfer (NEFT) Account No. : 676801700388 In name of "REGISTRAR (SPONSORED RESEARCH) MNIT Jaipur" Bank : ICICI Bank, Branch MNIT Jaipur IFSC Code: ICIC0006768. 2. Email filled in "Registration Form", scan copy of "Demand Draft/ NEFT Transaction Receipt" and pdf file (downloaded from GIAN Portal Registration) to gaurms@mnit.ac.in. Please mention "GIAN (Recent Advances in VLSI Testing) in Subject of the email.

The Faculty

Professor Adit Singh is James B. Davis Professor at Auburn University since 2002. He is an IEEE fellow and leading expert on VLSI testing. He is widely recognized as a pioneer in the area of adaptive testing. Over the past two decades, he has published and lectured widely on the subject. He has presented tutorials on the topic at practically every major test and design automation conference in the world, including at the flagship IEEE International Test Conference every year for the past 10 years. He has served as a consultant to most of the major semiconductor companies, and holds international patents in the test field that have been licensed to industry. He has been receipient of many awards including Walker Merit Teaching Award (2004), College of Engineering, Auburn University; Fulbright Award (1999) and Max-Planck Research Award (1998), Germany. His research interests are VLSI Design, Integrated Circuit Testing, Microelectronic Reliability, Nanoelectronics.

Dr. M.S.Gaur is a Professor at Computer Science and Engineering Department of Malaviya National Institute of Technology Jaipur. His research interests include information security and NoC (Networks on Chip). He has obtained his B.E. (JNV University , 1988), M.E. (IISc, 1992) and PhD (from University of Southampton, UK, 2004). He has guided 14 PhDs and has 150 publications in Journals and Conferences. He has coordinated national and international projects in the domains of Information Security and Networks on Chip. He is a member of IEEE, ACM, VLSI Society of India.

Dr. Lava Bhargave is currently an Associate Professor at Electronics and Communication Engineering Department, Malaviya National Institute of Technology Jaipur, India. His research interests are in the areas of Low power VLSI systems, VLSI physical design, FPGAs. He has been associated with Phase II of VLSI-SMDP (Special Manpower Development Project in VLSI & related project and ICT Academy at MNIT Jaipur. He has published several research articles in various conferences and journals. He has served as TPC member in many International conferences. He is a member of ACM, IEEE and IETE.

Course Coordinators

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