Advanced Digital Video Coding Standards

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Overview

High Efficiency Video Coding (HEVC) is the latest Video Coding format. It challenges the state-of-the-art H.264/AVC Video Coding standard which is in current use in the industry by being able to reduce the bit rate by 50% and yet retaining the same video quality. It came into existence in the early 2012 although Joint Collaborative Team on Video Coding (JCT-VC) was formed in January 2001 to carry out developments on HEVC, and ever since then a huge range of development has been going on. On 13 April 2013, HEVC standard also called H.265 was approved by ITU-T. (JCT-VC) is a group of video coding experts from ITU-T Study Group (VCEG) and ISO/IEC JTC 1/SC 29/WG 11 moving picture experts group (MPEG). HEVC is designed to address existing applications of H.264/MPEG-4 AVC and to focus on two key issues: increased video resolution and increased use of parallel processing architectures. It primarily targets consumer applications as pixel formats are limited to 4:2:0 8-bit and 4:2:0 10-bit. Main, Main 10 and Main intra profile (Main Still Picture profile) were finalized in 2013. The next revision of the standard, in July 2014, has enabled new use-cases with the support of additional pixel formats such as 4:2:2 and 4:4:4 and bit depth higher than 10-bit, embedded bit-stream scalability and 3D and multi-view video. Some other extensions such as Screen Content Coding (SCC) have been finalized in 2016. Preliminary work has already started on beyond HEVC. Several companies and research institutes have developed custom software for HEVC codecs and are actively working on hardware implementation of HEVC encoders/decoders. Some companies have developed HEVC decoders (FPGA, VLSI, SOC etc.).

An increasing diversity of services, the growing popularity of HD video, and the emergence of beyond-HD formats (e.g., 4K×2K or 8K×4K resolution) are creating even stronger needs for coding efficiency superior to H.264/MPEG-4 AVC's capabilities. HEVC is designed to address the increased video traffic and increased resolution such as the 4K and 8K videos.

This course is organized in ten modules that should be taken together. The topics in Module 1 will expose the participants to the Digital representation of video and Basics of Image / Video Compression. Modules 2 and 3 will discusses about some of the well-known video compression standards such as H.264/MPEG-4 Part -10 advanced video coding (AVC) , AVS China (IEEE 1857.4) and DAALA. Module 4 discusses one of the latest video compression standard, High efficiency video coding (HEVC) in detail and in Module 5, HEVC Extensions: MVC/3D , SCC, SVC, MPEG – systems are emphasized. Module 6 focuses on VP8, VP9 and VP10 video coding standards (Google) and ATSC (FCC).In Module 7, Image coding using JPEG, JPEG LS, JPEG 2000, JPEG-XR, JPEG-X and JPEG-Pleno will be discussed. Module 8 gives an introduction to Transcoders, Audio / Video Multiplex / De-multiplex/lip sync. Module 9 explains about SMPTE: VC1, VC2, DIRAC and Module 10 discuss about the different performance metrics such as PSNR, MOS, SSIM, BD bitrate, BD PSNR.

Course participants will learn these topics through lectures and hands-on experiments. Also case studies and assignments will be shared to stimulate research motivation of participants.

Modules	
	1: Digital representation of video, Basics of Image / Video Compression : January 1, 2018
	2: H.264/MPEG-4 Part -10 advanced video coding (AVC) : January 2, 2018
	3: AVS China (IEEE 1857.4), DAALA : January 3, 2018
	4: High efficiency video coding (HEVC) : January 4, 2018
	5: HEVC Extensions: MVC/3D , SCC, SVC, MPEG – systems : January 5, 2018
	6: VP8, VP9 and VP10 video coding standards (Google), ATSC (FCC) : January 8, 2018
	7: Image coding using JPEG, JPEG LS, JPEG 2000, JPEG-XR, JPEG-XT, JPEG-Pleno : January 9, 2018
	8: Transcoders, Audio / Video Multiplex / De-multiplex/lip sync : January 10, 2018
	9: SMPTE: VC1, VC2, DIRAC : January 11, 2018

	10: Performance Metrics: PSNR, MOS, SSIM, BD bitrate, BD PSNR, implementation complexity, Beyond HEVC : January 12, 2018 **Number of participants for the course will be limited to 30.**
You Should Attend If…	• You are a Computer Engineer or research scientist interested in data compression. • You are a student or a faculty member from Department of Computer Science and Engineering, Electronics and Communication or Information Technology. • You are a student or a faculty member from academic institution interested in learning how to do research on video compression or wants to work with compression for industries.
Fees	The participation fee for taking the course is as follows: **Participants from abroad : USD 400** **Industry/ Research Organizations: INR 8000** **Academic Institutions: INR 5000** **Students/Research Scholars: INR 3000** The above fee includes all instructional materials, computer use for tutorials and assignments, laboratory equipment usage charges and free internet facility. The participants will be provided with accommodation on payment basis.

The Faculty

K. R. Rao received the Ph. D. degree in electrical engineering from The University of New Mexico, Albuquerque in 1966. He is now working as a professor of electrical engineering in the University of Texas at Arlington, (UTA) Texas. He has published (coauthored) 19 books, some of which have been translated into Chinese, Japanese, Korean, Russian and Spanish. Also as e-books and paper back (Asian) editions. He has supervised 113 Masters and 31 doctoral students. He has published extensively and conducted tutorials/workshops worldwide. He has been a visiting professor in National university of Singapore and electronics and telecommunications research institute (ETRI) , Taejon, Korea. He has been a keynote speaker in many national and international conferences. He has been a consultant to academia, industry and research institutes. He has been an external examiner for several M.S. and Ph. D. students worldwide. He has been a reviewer of research proposals from Brazil, China, India, Korea, Singapore, Taiwan, Thailand and US. He was invited to review applications for recruitment and/or promotion of faculty in various Universities (US and abroad). He is an IEEE Fellow. He has been a member of the academy of distinguished scholars, UTA.

http://www.uta.edu/faculty/krrao/dip/

https://en.wikipedia.org/wiki/K._R._Rao

Dr. Madhu S. Nair received his Bachelors Degree in Computer Applications (B.C.A.) from Mahatma Gandhi University with First Rank in the year 2000, Masters Degree in Computer Applications (M.C.A.) from Mahatma Gandhi University with First Rank in the year 2003 and Masters Degree in Technology (M.Tech.) in Computer Science (with specialization in Digital Image Computing) from University of Kerala with First Rank in the year 2008. He obtained his Ph.D. in Computer Science (Image Processing) from Mahatma Gandhi University in the year 2013. He also holds a Post Graduate Diploma in Client Server Computing (PGDCSC) from Amrita Institute of Computer Technology. He had also qualified National Eligibility Test (NET) for Lectureship conducted by University Grants Commission (UGC) in the year 2004 and Graduate Aptitude Test in Engineering (GATE) conducted by Indian Institute of Technology (IIT) in the year 2006. He has published around 70 research papers in reputed International Journals and Conference Proceedings published by IEEE, Springer, Elsevier, Wiley, IOS Press etc. He is a Senior Member of Institute of Electrical and Electronics Engineers (IEEE), Member of Association for Computing Machinery (ACM), Associate Life Member of Computer Society of India (CSI) and Member of International Association of Engineers (IAENG). He is a recipient of various prestigious awards.

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Course Coordinator

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